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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/726,042	12/01/2003	Nikhil V. Kelkar	NSC1P284	2661

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EXAMINER	
NGUYEN, DAO H	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 02/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/726,042	KELKAR ET AL.	
	Examiner	Art Unit	
	Dao H. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 November 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4,6-8,10-12,14,15 and 21-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4, 6-8, 10-12, 14, 15, and 21-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. *1105*.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. In response to the communications dated 11/17/2005, claims 1-4, 6-8, 10-12, 14, 15, and 21-25 are active in this application.

Claims 21-25 are newly added claims.

Claims 5, 9, 13, and 16-20 have been cancelled.

Remarks

2. Applicant's argument(s), filed 11/17/2005, with respect to claims 1-4, 6-8, 10-12, 14, 15, and 21-25 have been fully considered.

First, Applicant is notified that no allowability has been priorly indicated.

Second, Examiner agree(s) with Applicant that neither Huang nor Chien teaches an integrated circuit device having both a passivation layer and a resilient layer dipsoded atop the passivation layer. However, Chien does teach a semiconductor contact pad structure comprising contact pad 113 having under bump metallization stack 132 form thereon, wherein each under bump metallization stack 132 including a nickel-vanadium layer 130b and a copper layer 130a. Such teaching is clearly shown in figs. 5; and Applicant had no argument(s) about that. Accordingly, such teaching is used again to make rejection(s) in combination, or/and in addition, to the newly discovered references to Bojkov et al. (U.S. Patent Application Publication No.

2003/0116845), to Lee et al. (U.S. Patent Application Publication No. 2002/0121692), and/or to Kao et al. (U.S. Patent No. 6,249,044).

Claim Objections

3. The claim is objected to for the following remarks. Claims 6 and 7 depend on cancelled claim 5. Therefore, Applicant is required to make appropriate corrections to the dependencies of these claims.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claim(s) 8 is rejected under 35 U. S. C. § 102 (e) as being anticipated by U.S. Patent Application Publication No. 2003/0116845 by Bojkov et al.

Regarding claim 8, Bojkov discloses an integrated circuit device, as shown in fig. 5, comprising:

a plurality of contact pads 501 formed on a first surface of said device;

a passivation layer 503 disposed on said first surface, said passivation layer 503 including a plurality of passivation layer vias formed therethrough and associated with at least a portion of said plurality of contacts pads 501;

a resilient layer 506 defining a substantially horizontal plane and disposed on said passivation layer 503, said resilient layer 506 having a plurality of resilient layer vias formed therethrough and associated with at least a portion of said plurality of contact pads 501 and at least a portion of said plurality of passivation layer vias, wherein one or more of said plurality of resilient layer vias defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and contains one or more sidewalls that are not substantially parallel to said primary axis; and

a plurality of under bump metallization stacks 507/508, wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad 501, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers 507/508 (of copper, see paragraph [0039]), none of the layers 507/508 are an aluminum layer, a titanium layer or a chromium layer.

6. Claim(s) 8, 10, 12, 14, 15, and 21-25 are rejected under 35 U. S. C. § 102 (b) as being anticipated by U.S. Patent Application Publication No. 2002/0121692 by Lee et al.

Regarding claim 8, Lee discloses an integrated circuit device, as shown in figs. 1-4, comprising:

a plurality of contact pads 14 formed on a first surface of said device;

a passivation layer 12 disposed on said first surface, said passivation layer 12 including a plurality of passivation layer vias 19 formed therethrough and associated with at least a portion of said plurality of contacts pads 14;

a resilient layer 16 defining a substantially horizontal plane and disposed on said passivation layer 12, said resilient layer 16 having a plurality of resilient layer vias 21 formed therethrough and associated with at least a portion of said plurality of contact pads 14 and at least a portion of said plurality of passivation layer vias 19, wherein one or more of said plurality of resilient layer vias 21 defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and contains one or more sidewalls that are not substantially parallel to said primary axis; and

a plurality of under bump metallization stacks 18/20, wherein one or more of said plurality of under bump metallization stacks each couple with an associated contact pad 14, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers 18/20. Lee also teaches that layer 20 is a copper or nickel layer (page 2, paragraph [0014], layer 18 is a UBM layer of metal (page 2, paragraph [0013]), and furthermore, the UBM layer is typically of nickel (page 6, paragraph [0093]). Thus, it is clear that the under bump metallization stack can be formed by a plurality of metal or alloy layers, wherein none of the layers are an aluminum layer, a titanium layer or a chromium layer. (Note that though aluminum layer, titanium layer, or/and chromium layer can be used for the under bump metallization stack of Lee, but they are not the only materials that can be used; neither they are the materials that must be used.)

Regarding claim 10, Lee discloses the integrated circuit device wherein at least a portion of said plurality of under bump metallization stacks each comprise at least one layer selected from the group consisting of copper and nickel-vanadium (copper is selected in this case).

Regarding claim 12, Lee discloses the integrated circuit device wherein one or more of said plurality of under bump metallization stacks has a total thickness of less than about 15 kilo-angstroms. See page 2, paragraph [0014]; page 6, paragraph [0093].

Regarding claim 14, Lee discloses the integrated circuit device wherein one or more of said plurality of passivation layer vias 19 each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via 21, such that an associated under bump metallization stack 18/20 contacts said resilient layer 16 but does not contact said passivation layer 12. See figs. 1-4.

Regarding claim 15, Lee discloses the integrated circuit device further comprising a plurality of solder bumps 22, wherein one or more of said plurality of solder bumps 22 are each coupled with an associated under bump metallization stack and an associated contact pad 14. See figs. 1-4.

Regarding claim 21, Lee discloses the integrated circuit device wherein said resilient layer 16 completely covers all top and side surfaces of said passivation layer 12 at lat least a portion of said plurality of passivation layer vias 19. See figs. 1-4.

Regarding claim 22, Lee discloses the integrated circuit device wherein said passivation layer 12 comprises a silicon based material. See paragraph [0074]

Regarding claim 23, Lee discloses the integrated circuit device wherein said passivation layer 12 comprises one or more materials selected from the group consisting of SiO_2 and SiN. See paragraph [0074].

Regarding claim 24, Lee discloses the integrated circuit device wherein said resilient layer 16 comprises benzocyclobutene or a polyimide. See paragraph [0071].

Regarding claim 25, Lee discloses an integrated circuit device, as shown in figs. 1-4, comprising:

a plurality of contact pads 14 formed on active surface of said device;

an inoraginc passivation layer 12 (see paragraph [0074]) disposed upon said active surface, said passivation layer 12 including a plurality of passivation layer vias 19 formed therethrough and associated with at least a portion of said plurality of contacts pads 14;

a polymeric resilient layer 16 (see paragraph [0071]) defining a substantially horizontal plane and disposed upon and substantially covering said passivation layer 12, said resilient layer 16 having a plurality of resilient layer vias 21 formed therethrough and associated with at least a portion of said plurality of contact pads 14 and at least a portion of said plurality of passivation layer vias 19, wherein one or more of said plurality of resilient layer vias 21 defines a primary axis extending therethrough and perpendicular to said substantially horizontal plane, and contains one or more sidewalls that are not substantially parallel to said primary axis; and

a plurality of under bump metallization stacks 18/20, wherein one or more of said plurality of under bump metallization stacks 18/20 each couple with an associated contact pad 14, and wherein each such under bump metallization stack comprises a plurality of metal or alloy layers 18/20, none of which are an aluminum layer, a titanium layer or a chromium layer (layer 20 is a copper or nickel layer (page 2, paragraph [0014], layer 18 is a UBM layer of metal (page 2, paragraph [0013]), and furthermore, the UBM layer is typically of nickel (page 6, paragraph [0093]). Thus, it is clear that the under bump metallization stack can be formed by a plurality of metal or alloy layers, wherein none of the layers are an aluminum layer, a titanium layer or a chromium layer. Note that though aluminum layer, titanium layer, or/and chromium layer can be used for the under bump metallization stack of Lee, but they are not the only materials that can be used; neither they are the materials that must be used.), and wherein one or more of said plurality of passivation layer vias 19 each define a perimeter that completely encloses the perimeter of a corresponding resilient layer via 21, such that an associated

under bump metallization stack 18/20 contacts said resilient layer 16 but does not contact said passivation layer 12; and

a plurality of solder bumps 22, wherein one or more of said plurality of solder bumps 22 are each coupled with an associated under bump metallization stack and an associated contact pad 14.

Claim Rejections - 35 U.S.C. § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim(s) 1-4, and 6 are rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,249,044 to Kao et al., in view of U.S. Patent No. 6,258,705 to Chien et al.

Regarding claim 1, Kao discloses a semiconductor wafer having an active surface, as shown in figs. 2, 3C comprising:

a plurality of dice, each die having a plurality of contact pads 32 formed on the active surface of the wafer 31;

a passivation layer 33 disposed on said active surface, said passivation layer 33 having a plurality of passivation layer vias 34 formed therethrough and associated with at least a portion of said plurality of contacts pads 32;

a resilient layer 35 disposed on said passivation layer 33, said resilient layer 35 having a plurality of resilient layer vias 36 formed therethrough, wherein sidewalls of at least some of said plurality of resilient layer vias 36 are tapered at an angle relative to the active surface of said die;

a plurality of under bump metallization stacks 37 (or 37A/B), each under bump metallization stack including a first layer 37A and a second layer 37B, wherein the first layer 37A is directly atop and in substantial contact with an associated contact pad 32 and the second layer 37B is directly atop and in substantial contact with the first layer 37A, said under bump metallization stack being arranged such that at least some portion of the under bump metallization stack overlies a portion of said resilient layer 35; and

a plurality of solder bumps 21, each solder bump being formed on an associated under bump metallization stack 37A/B.

Though in the shown fig. 3C, the first layer 37A is of chromium, and the second layer 37B is of copper-chromium (see col. 4, lines 43-46), Kao further teaches in col. 4, line 64 to col. 5, line 9 that materials other than those named in the preferred embodiments can be used in each of the parts enumerated in fig. 3(A-D); that the under bump layer 37 may be formed of layers of any suitable conductive materials.

Chien discloses a semiconductor contact pad structure, as shown in figs. 5, comprising contact pad 113 having under bump metallization stack 132 form thereon, wherein each under bump metallization stack 132 including a nickel-vanadium layer 130b and a copper layer 130a.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made that suitable conductive materials for the under bump layer can be a stack of a nickel-vanadium layer and a copper layer as that described by Chien; Hence, one of skills in the art can obviously modify the invention of Kao to have an under bump metallization stack wherein the first layer is a nickel-vanadium layer and the second layer is a copper layer, as that of Chien, since selecting a known material on the basis of its suitability for the intended use is just within the general skill of a worker in the art. In re Leshin, 125 USPQ. In addition, the benefit of such modification is to obtain a cost-effective device (see col. 4, lines 55-63 of Chien).

Regarding claim 2, Kao/Chien discloses the semiconductor device, wherein said resilient layer comprises a polyimide. See col. 4, lines 27-29 of Kao.

Regarding claims 3, 4, Kao/Chien discloses the semiconductor/integrated device comprising all claimed limitations. See also col. 4, lines 24-36 of Kao; and col. 5, lines 44-52 of Chien.

Moreover, it would have been an obvious to one of ordinary skills in the art that the thickness of such stack can be chosen modified at any suitable value, depending on the desired device, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. In re Rose, 105 USPQ 237 (CCPA 1955).

Regarding claim 6, Kao/Chien discloses the semiconductor device, wherein said passivation layer comprises a compound selected from the group consisting of silicon dioxide and silicon nitride. See col. 4, lines 24-28 of Kao.

9. Claim(s) 7 is rejected under 35 U.S.C. 103 (a) as being unpatentable over U.S. Patent No. 6,249,044 to Kao et al., in view of U.S. Patent No. 6,258,705 to Chien et al., and further in view of U.S. Patent Application Publication No. 2002/0121692 by Lee et al.

Regarding claim 7, Kao/Chien discloses the semiconductor device comprising all claimed limitations, except for each of said plurality of passivation layer vias defining a perimeter that completely enclosing the perimeter of a corresponding resilient layer via.

Lee discloses a contact pad structure, as shown in figs. 1-4, having contact pads 14, a passivation layer 12 disposed on the contact pads 14 and having passivation vias 19, and a resilient layer 16 disposed on the passivation layer 12 and having resilient

vias 21; wherein each of the passivation layer vias 19 defining a perimeter that completely enclosing the perimeter of a corresponding resilient layer via 21.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the invention of Kao/Chien so that the passivation layer vias and the resilient layer vias having perimeters as those of Lee. The motivation of such modification is to obtain a contact pad structure wherein the silicon dioxide passivation layer being covered by the polyimide resilient layer to prevent copper from the under bump metallization stacks diffusing into the silicon dioxide passivation layer. See paragraph [0079] of Lee.

Conclusion

10. **THIS ACTION IS MADE FINAL.** A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dao Nguyen whose telephone number is (571)272-1791. The examiner can normally be reached on Monday-Friday 9:00am - 6:00pm. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms, can be reached on (571)272-1787. The fax numbers for all communication(s) is (571)273-8300.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571)272-1625.

David Nelms
Supervisory Patent Examiner
Technology Center 2800

Dao H. Nguyen
Art Unit 2818
February 8, 2006